

[0080] Such a configuration enables a layout area to be reduced.

Seventh Embodiment

[0081] The present embodiment is described with reference to FIG. 14. In FIG. 14, the present embodiment is different from the fifth embodiment in that the region where the first electrode 13 is arranged and the region where the second electrode 26 is arranged are arranged not on a row basis, but in a checkered pattern.

[0082] According to such a configuration, fixed state of potential on the buried layer 2 and the potential barrier 6 is not weakened as compared to the fixed state in the fifth embodiment. Furthermore, it is enabled to prevent problems with a sensitivity ratio between the same color pixels from being caused because two green pixels are equal to each other in shape when a color filter is arranged in a Bayer color array in the pixel region.

[0083] As described above, according to the solid-state imaging apparatus of the present invention, even when the VOFD function is used to realize the electronic shutter function, variation in the amount of accumulated carriers in the carrier accumulation region is reduced to permit a high image-quality photographing.

[0084] In the above embodiments, although a description is made with an electron as a carrier, it is not limited to an electron. The above effect and operation can be achieved even with a hole as a carrier. In that case, a potential may be properly reversed.

[0085] In the above embodiments, although there is described an example where the control gate of the carrier accumulation region is formed of a double layered polysilicon, the gist of the present invention is to provide the carrier accumulation region, so that the control gate of the carrier accumulation region may be formed of a plural (two or more) layered poly-silicon or single layered poly-silicon, for example.

[0086] The present invention is not limited to the above embodiments, and further modifications and combinations can be made without departing from the spirit of the present invention.

[0087] According to the present invention, even when the VOFD function is used, variation in the amount of accumulated carriers is reduced to permit a high image-quality photographing.

[0088] While the present invention has been described with reference to exemplary embodiments, it is to be understood that the invention is not limited to the disclosed exemplary embodiments. The scope of the following claims is to be accorded the broadest interpretation so as to encompass all such modifications and equivalent structures and functions. This application claims the benefit of Japanese Patent Application No. 2008-101560, filed Apr. 9, 2008, which is hereby incorporated by reference herein in its entirety.

What is claimed is:

1. A solid-state imaging apparatus having a semiconductor substrate of a first conductivity type, and a plurality of pixels arranged in a pixel region of the semiconductor substrate, each pixel including a photoelectric conversion region and an amplifying transistor for amplifying a signal based on a signal carrier generated in the photoelectric conversion region and for outputting an amplified signal, performing a vertical over flow drain operation, wherein the pixel region includes:

- a first semiconductor region of the first conductivity type for forming a part of the photoelectric conversion region;
 - a second semiconductor region of the first conductivity type for accumulating the carriers generated in the photoelectric conversion region;
 - a third semiconductor region of a second conductivity type arranged under the second semiconductor region, as a potential barrier holding the accumulated carriers in the second semiconductor region;
 - a fourth semiconductor region of the second conductivity type extending between the first semiconductor region and the semiconductor substrate, and between the third semiconductor region and the semiconductor substrate; and
 - a first voltage supply portion for supplying a reference voltage to the third semiconductor region, and the first voltage supply portion includes a fifth semiconductor region of the second conductivity type arranged in the pixel region, and a first electrode connected to the fifth semiconductor region.
2. The solid-state imaging apparatus according to claim 1, wherein
- a plurality of the first voltage supply portions are arranged in the pixel region.
3. The solid-state imaging apparatus according to claim 1, wherein
- the amplifying transistor has source and drain regions arranged in a well of the second conductivity type, and the well is electrically connected to the third semiconductor region.
4. The solid-state imaging apparatus according to claim 1, further comprising
- a floating diffusion region of the first conductivity type connected to a gate of the amplifying transistor, and the third semiconductor region extends under the source and drain of the amplifying transistor.
5. The solid-state imaging apparatus according to claim 1, wherein
- the fifth semiconductor region is arranged in an active region adjacent to an active region in which the second semiconductor region is arranged, and an isolation region is sandwiched between the active region in which the fifth semiconductor region is arranged and the active region in which the second semiconductor region is arranged.
6. The solid-state imaging apparatus according to claim 1, further comprising
- a floating diffusion region of the first conductivity type connected to a gate of the amplifying transistor, and the fifth semiconductor region is arranged in an active region adjacent to an active region in which the floating diffusion region is arranged, and an isolation region is sandwiched between the active region in which the fifth semiconductor region is arranged and the active region in which the floating diffusion region is arranged.
7. The solid-state imaging apparatus according to claim 1, wherein
- the fifth semiconductor region is arranged in an active region adjacent to an active region in which the amplifying transistor is arranged, and an isolation region is sandwiched between the active region in which the fifth semiconductor region is arranged and the active region in which the amplifying transistor is arranged.